RAMAKRISHNA MISSION VIDYAMANDIRA

(Residential Autonomous College under University of Calcutta)

B.A./B.SC. FIRST SEMESTER EXAMINATION, DECEMBER 2012

FIRST YEAR

Date : 21/12/2012 **ELECTRONICS (General)**

Time : 11 am – 1 pm Paper : I Full Marks : 50

Answer **any five** questions :

1. Answer the following : [5×2]
   a) Find the Gray Codes of the following binary numbers—
      i) 11001100
      ii) 01011110
   b) Find the addition of the following decimal numbers in BCD(8421) :
      i) 15 + 24
      ii) 19 + 22
   c) Convert the following decimal numbers to their hexadecimal equivalents :
      i) $(214)_{10}$
      ii) $(214 \cdot 356)_{10}$
   d) If $(257)_{10} = (401)_x$, determine the value of x.
   e) Why is a priority encoder preferred over a normal encoder?

2. a) State and prove De Morgan's Theorem for two variables.
   b) Minimize the following logic functions using K-map.
      i) $f(A,B,C,D) = \sum m(0,1,2,3,5,7,8,9,11,14)$
      ii) $f(A,B,C,D) = \Pi M(4,6,10,12,13,15)$ [4+(3+3)]

3. a) Distinguish between Combinational and Sequential Logic Circuit.
   b) Design an 8:1 multiplexer with two 4:1 multiplexers.
   c) Mention the applications of a multiplexer. [3+4+3]

4. a) "A decoder can be used as a demultiplexer." —Explain.
   b) Explain the operation of a 2:4 decoder and hence draw the logic circuit of the same using NAND gates only. [4+6]

5. a) What is the Race-around Condition? How is it overcome in a Master – slave J-K flip-flop?
   b) Draw the circuit of a D-flip flop using logic gates and explain its operation. [2+5+3]

6. a) Design a MOD-5 synchronous Counter using J-K Flip-Flop with proper Excitation & State Table.
   b) Explain the operation of a 4-bit shift register. [7+3]

7. Write short notes on <u>any two</u> of the following : [5×2]
   a) Synchronous & Asynchronous Counters.
   b) NAND gate as a universal Logic gate
   c) Half and full adders
   d) SR flip flop

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